

REMARKS

Claims 1-23 are pending. All of the claims stand rejected. The independent claims are claims 1 and 13. The Office Action indicates that claims 1-21 are rejected as obvious from *Takahashi* in view of a new reference: *Lemaguet* (U.S. Patent No. 6,314,138) having a July 21, 1998 priority date. Additionally, the Office Action rejects claims 22-23 based upon the two same references, and in further view of *Bock* (WO 97/47128) having priority date June 3, 1996. Claims 22-23 depend from independent claims 1 and 13 respectively.

The Office Action states that Figure 5 of *Lemaguet* teaches the feature of separating different types of data in the encoded digital video bitstream, including virtual buffer verifier values. This was the limitation that Applicant added to claims 1 and 13 on September 21, 2004. Applicant respectfully disagrees that *Lemaguet* teaches or suggests this feature.

Figure 5 of *Lemaguet* is relied upon by the Examiner, and that Figure 5 is described at column 4, lines 17-32 of *Lemaguet*. The arrangement shown in Figure 5 of *Lemaguet* shows the internal structure of each transcoder 11 and 12 in *Lemaguet*'s Figure 1.

It is very useful to compare Figure 5 of *Lemaguet* to Figure 5 of the present application. *Lemaguet*'s Figure 5 only shows two paths from the input to the output. In contrast, Figure 5 of the present application shows a much more elaborate set of paths. The first branch of *Lemaguet* includes elements 51-56, and this branch is somewhat similar to the branch of present Figure 5 that includes elements 505-508. The second branch of *Lemaguet* includes element 57 in order to introduce a delay, and that second branch is somewhat similar to the "untouched" path in present Figure 5, as explained in the present application at page 15, lines 7-20 (block 503 receives synchronization information from block 502 to preserve "temporal relations"). Thus, there is no branch in *Lemaguet*'s Figure 5 corresponding to the path through element 509 of the present Figure 5, or through element 510 of the present Figure 5. It is the path through present element

510 that is claimed by the last “wherein” clause of present claim 1. Figure 5 of *Lemaguet* does not show anything like this.

The examiner acknowledges (page three, last paragraph) that *Takahashi* fails to disclose a bitstream analyzer. However, Figure 5 of *Lemaguet* also fails to disclose a bitstream analyzer for separating different types of data, much less for separating virtual buffer verifier values as presently claimed. *Lemaguet* does not teach or suggest that the bitstream flowing into delay element **57** is any different from the bitstream flowing into variable length decoder element **51**, and thus *Lemaguet* does not disclose anything comparable to the bitstream analyzer **502** of the present claimed invention.

The Office Action points to the branch formed by the delay line **57** in Figure 5, but that branch merely introduces a delay equal to a transcoding delay. There is no indication in *Lemaguet* that the branch having the delay line **57** does anything other than introduce a delay. *Lemaguet* does not mention anything about separating virtual buffer verifier values, either with regard to Figure 5 or with regard to any of the other figures in that patent.

As mentioned, the arrangement shown in Figure 5 of *Lemaguet* shows the internal structure of each transcoder **11** and **12** in *Lemaguet*’s Figure 1. Each of those transcoders performs a very simple function, unrelated to bitstream analysis, and unrelated to separating different types of data.

If *Lemaguet* had realized the usefulness of separating virtual buffer verifier values, then he would have put a bitstream analyzer at the branching point prior to the variable length decoder, as shown in present Figure 5. Instead, *Lemaguet* has put a bitstream analyzer nowhere. For this reason, Applicant respectfully submits that the present independent claims should be allowed, and it is unnecessary to address the allowability of the dependent claims.

The characteristics of the bitstream analyzer of the present invention are described in the description of Fig. 5 beginning at page 8 of the present application:

“A bit stream analyzer block **502** is coupled to the input **501**. It has four data outputs which are known as the ‘*untouched*’ output, ‘DCT coefficients’ output, ‘quantization matrices’ output and the ‘*virtual buffer verifier*’ output. Additionally, the bit stream analyzer block **502** has a

control output. . . . The bit stream analyzer block **502** performs a demultiplexing function where the *VBV* values and other *virtual buffer* related information are directed to the *VBV* value modifier block **510**, the weighting (quantization) matrices are directed to the element-wise matrix multiplier block **509**, the DCT coefficient matrices are directed to the variable length decoder **505** and the rest of the bitstream is directed through the ‘*untouched*’ output to the corresponding input of the multiplexer block **503**.”

Applicant notes that the primary embodiments in *Takahashi* (the first and second embodiments) suggest data reduction to be achieved at the level of the actual video image information. *Takahashi* has probably adopted the idea of handling the whole information, and therefore has never come across the idea of using a bitstream analyzer to separate the different kinds of data from each other. In the Applicant's invention, there is a bitstream analyzer (block **502** in FIG. 5) that separates the original video stream into as many as four different component streams, which are the untouched data component stream, the DCT coefficients component stream, the weighing matrices component stream, and the *VBV* component stream. Clearly, *Lemaguet* discloses no more than two component streams, and those two component streams do not include a *VBV* component stream as claimed in present claims 1 and 13.

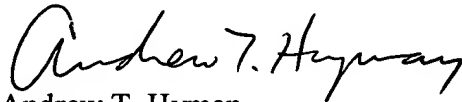
The mere fact that *Lemaguet* teaches an arrangement for processing MPEG video bitstreams and for calculating transport delay using *VBV* values does not in any way suggest that the *VBV* values are separated into a component stream by a bitstream analyzer. In *Lemaguet*, the *VBV* values are used to compute transcoding delay, for use by a delay element **57**. In contrast, the *VBV* values of the present invention are used to modify *VBV* values within the output signal, so as to properly reflect the reduction in the amount of bits associated with the blocks **505-508** (see first paragraph on page 15 of application). Thus, present claim 1 discloses “separating” *VBV* values from other types of data, whereas *Lemaguet* suggests no need to “separate” the *VBV* values from the other types of data, as long as certain of those intermixed *VBV* values can be detected and therefore used to calculate the transport delay.

CONCLUSION

Applicants respectfully submit that the claims of the present application define patentable subject matter and are patentably distinguishable over the cited references for the reasons explained. The rejections of the non-final Official Action of 3 November 2004 having been shown to be inapplicable, retraction thereof is requested, and early passage of all the pending claims to issue is earnestly solicited.

Applicant would appreciate if the Examiner would please contact Applicant's attorney by telephone, if that might help to speedily dispose of any unresolved issues pertaining to the present application.

Respectfully submitted,



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